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09/989,777	11/19/2001	Craig Nemecek	CYPR-CD01208M	2046

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WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
SHARON, AYAL I	
ART UNIT	**PAPER NUMBER**
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No. 09/989,777	Applicant(s) NEMECEK, CRAIG	
	Examiner Ayal I. Sharon	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. Claims 1-28 of U.S. Application 09/989,777 filed on 11/19/2001 are presented for examination.

Drawings

2. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.
3. Figs. 6 and 7 are objected to for being illegible and having a font size that is too small to read.

Oath/Declaration

4. Examiner reminds the Applicant that the Declaration includes a statement that the person making the oath or declaration acknowledges the duty to disclose to the Office all information known to the person to be material to patentability as defined in 37 CFR 1.56.
5. Examiner notes that the specification of the instant application does not make any mention of applicant's numerous co-pending applications.

6. Moreover, Examiner found relevant prior art, including prior art that Examiner has applied in art rejections in the instant application, in applicant's co-pending applications 09/975,105 and 10/004,039. Applicant did not disclose this relevant prior art in the instant application.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

   A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

   Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1, 7, 10, 16, 21, and 25 are provisionally rejected under the judicially created doctrine of double patenting over the recently allowed (but not yet issued):

   a. Claim 1 of co-pending Application No. 09/998,834

   b. Claim 4 of co-pending Application No. 09/998,859

   In addition, Independent Claims 1, 7, 10, 16, 21, and 25 are also provisionally rejected under the judicially created doctrine of double patenting over the currently co-pending:

c. Claim 1 of co-pending Application No. 09/975,030

d. Claim 1 of co-pending Application No. 09/975,105

e. Claim 1 of co-pending Application No. 09/975,338

f. Claim 1 of co-pending Application No. 09/992,076

g. Claim 1 of co-pending Application No. 10/001,477

h. Claim 1 of co-pending Application No. 10/001,478

i. Claim 1 of co-pending Application No. 10/001,568

j. Claim 1 of co-pending Application No. 10/004,039

k. Claim 1 of co-pending Application No. 10/004,197

These are provisional double patenting rejections, since the conflicting claims have not yet been patented.

9. The subject matter claimed in the instant application is fully disclosed in the referenced co-pending applications and would be covered by any patent granted on that co-pending application since the referenced co-pending application and the instant application are claiming common subject matter, as follows:

a. Claim 1 of co-pending Application No. 09/998,834 claims, includes the following limitations:

> ... a debug interface included in the microcontroller for communicatively coupling the microcontroller and the ICE, the interface configured to enable data transmission when the microcontroller is operating at a first speed and to disable data transmission when the microcontroller is operating at a second speed, wherein said first speed is slower than said second speed.

Examiner interprets that the " ... interface configured to disable data transmission ..." feature corresponds to the "turning off one or more clock", "discontinuing sending .. clock signals", "initiating said sleep function", "initiating said stall function", and "turning off said clock" limitations in the independent claims of the instant application.

b. Independent Claim 4 of co-pending Application No. 09/998,859 includes the following limitations:

> A system for checking the consistency of a lock-step process comprising: ...
>
> ... an interface for coupling the production microcontroller and the ICE enabling transmission of the first value to the ICE, where the production microcontroller sends to the ICE a result of an execution of a line of code, and wherein the ICE compares the first value against the second value.

Examiner interprets that these features corresponds to the "... emulating the functions of said device under test by operating in lock-step fashion with said device under test ..." and "... discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock ..." limitations in the independent claims of the instant application.

c. Claim 1 of co-pending Application No. 09/975,030 includes the following limitations:

> A communication interface for coupling a device (DUT) under test with an emulator device, the emulator device implementing the DUT and executing instructions in lock-step with the DUT, the communication interface comprising:

> ... a clock portion that supplies clock information to the DUT and the emulator device; wherein the time dependent data transport portion transports varying types of information depending upon an [sic] time phase of operation of the DUT and the emulator device.

Examiner interprets that these features corresponds to the "... emulating the functions of said device under test by operating in lock-step fashion with said device under test ..." and "... discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock ..." limitations in the independent claims of the instant application.

d. Claim 1 of co-pending Application No. 09/975,105 includes the following limitations:

> A method of programming a field programmable gate array (FPGA), comprising ...
>
> ... the host clocking configuration data over the data lines into the FPGA using the data strobe line to clock the configuration clock, the configuration data incorporating design parameters for the specified interface so that the FPGA, once programmed, incorporates the specified interface ...

Examiner interprets that these features corresponds to the "... emulating the functions of said device under test by operating in lockstep fashion with said device under test ..." and "... discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock..." limitations in the independent claims of the instant application.

e. Claim 1 of co-pending Application No. 09/975,338 includes the following limitations:

> A method of performing a breakpoint operation in an emulation system, comprising:
>
> ... in response to determining that a breakpoint is required, the emulator issues a halt command instructing the DUT to halt execution, and wherein both the emulator and the DUT halt execution at the same point within the set of instructions.

Examiner interprets that these features corresponds to the "... emulating the functions of said device under test by operating in lock-step fashion with said device under test ..." and "... turning off one or more clock [sic] of said device under test ..." and "... discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock ..." limitations in the independent claims of the instant application.

f. Claim 1 of co-pending Application No. 09/992,076 includes the following limitations:

> A system for debugging microcontroller code comprising:
>
> ... an interface for coupling the test circuit and the ICE enabling data transmission between the test circuit and the computer system, the computer system capable of comparing a content of the first memory against a content of the second memory to verify said lock step.

Examiner interprets that these features corresponds to the "... emulating the functions of said device under test by operating in lock-step fashion with said device under test ..." and "... discontinuing execution of

instructions that are performed in lock-step by said emulator device upon turning off said clock ..." limitations in the independent claims of the instant application.

g. Claim 1 of co-pending Application No. 10/001,477 includes the following limitations:

> An In-circuit Emulation system breakpoint control, comprising:
> a microcontroller;
> a virtual microcontroller operating in lock-step synchronization with the microcontroller;
> a breakpoint lookup table associated with the virtual microcontroller with a break bit associated with each of a plurality of instruction addresses, the break bit being set to indicate that a break is to occur at a specified instruction address; and
> a breakpoint controller that sends a break message to the microcontroller whenever an instruction address is encountered, that is associated with a set break bit.

Examiner interprets that these features corresponds to the "... emulating the functions of said device under test by operating in lock-step fashion with said device under test ..." and "... discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock ..." limitations in the independent claims of the instant application.

h. Claim 1 of co-pending Application No. 10/001,478 includes the following limitations:

> 1 . A boot method for an In-circuit Emulation system having a microcontroller operating in lock-step synchronization with a vidual microcontroller, comprising:
>
> in the microcontroller, executing a set of boot code;

> in the virtual microcontroller, executing a set of timing code timed to take the same number of clock cycles as the microcontroller uses to execute the boot code; and
>
> simultaneously halting both the microcontroller and the virtual microcontroller.

Examiner interprets that these features corresponds to the "... emulating the functions of said device under test by operating in lock-step fashion with said device under test ..." and "... discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock ..." limitations in the independent claims of the instant application.

i. Claim 1 of co-pending Application No. 10/001,568 includes the following limitations:

> A combined in-circuit emulation system and programmer, comprising:
>
> a pod carrying an emulation microcontroller and a socket for programming another microcontroller;
>
> a base station having virtual microcontroller that operates in lock-step synchronization with the emulation microcontroller during emulation operations;
>
> an interface connecting the pod to the base station, the interface having a clock signal line, a pair of data signal lines, a reset line and a power line, wherein the reset line is connected to the emulation microcontroller, but is not connected to the socket; and
>
> wherein the emulation microcontroller can be placed in a sleep mode so that a microcontroller residing in the socket can be programmed by receiving programming information from the base station without the programming being disturbed by actions of the emulation microcontroller.

Examiner interprets that these features corresponds to the "... emulating the functions of said device under test by operating in lock-step fashion

with said device under test ..." and "... discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock ..." limitations in the independent claims of the instant application.

j. Claim 1 of co-pending Application No. 10/004,039 includes the following limitations:

> An In-circuit Emulation system, comprising:
> a microcontroller having a microcontroller clock;
> a virtual microcontroller running in lock-step synchronization with the microcontroller;
> a host computer running In-circuit Emulation debug software, the host computer being in communication with the virtual microcontroller; and
> a gatekeeper circuit coupled to the virtual microcontroller and the microcontroller, the gatekeeper circuit detecting when a watchdog timer expires in the microcontroller and notifying the host computer that the watchdog event has occurred.

Examiner interprets that these features corresponds to the "... emulating the functions of said device under test by operating in lock-step fashion with said device under test ..." and "... discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock ..." limitations in the independent claims of the instant application, because a "watchdog event" corresponds to "turning off a clock".

k. Claim 1 of co-pending Application No. 10/004,197 includes the following limitations:

> An In-circuit Emulation system, comprising:
> a microcontroller having a microcontroller clock;

> a virtual microcontroller running in lock-step synchronization with the microcontroller;
> a gatekeeper circuit coupled to the virtual microcontroller and the microcontroller; and
> a host computer running In-circuit Emulation debug software, the host computer being in communication with the gatekeeper circuit so that halt commands requests for data from the virtual microcontroller are passed through and regulated by the gatekeeper circuit.

Examiner interprets that these features corresponds to the "... emulating the functions of said device under test by operating in lock-step fashion with said device under test ..." and "... discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock ..." limitations in the independent claims of the instant application, because a ".. halt commands requests for data ..." corresponds to "turning off a clock".

10. Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other co-pending application. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 21-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention. Examiner finds independent claims 21 and 25 to be incomprehensible. All dependent claims inherit this defect.

13. The examiner has made prior art rejections of these claims based on the scope of information contained in the specification, and based on the other claims in the instant application, which are assumed to be directed to the same invention.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. The prior art used for these rejections is as follows:

16. Profit. Jr., U.S. Patent 5,911,059. (Henceforth referred to as "**Profit**").

17. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

18. Claims 1-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Profit.

19. In regards to Claim 1,

> 1. For a system that includes a device under test and that includes an emulator device:
>
> a) emulating the functions of said device under test by operating in lock-step fashion with said device under test; and

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

b) performing a sleep operation, comprising:

b1) upon receiving a first signal that indicates that a sleep function is to be performed, initiating said sleep function at said device under test;

b2) turning off one or more clock of said device under test; and

b3) discontinuing execution of instructions that are performed in lock-step by said emulator device upon turning off said clock.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

20. In regards to Claim 2,

2. The method of Claim 1 wherein said clock comprises an internal CPU clock.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

21. In regards to Claim 3,

> 3. The method of Claim 2 wherein said first signal is generated by said device under test and is transmitted internally to a register that indicates that a sleep function is to be performed.

Examiner finds that the memory (Fig.7, Item 206) corresponds to claimed register. See col.12, lines 4-11 for more details.

22. In regards to Claim 4,

> 4. The method of Claim 1 further comprising:
>
> when said sleep function has been completed by said device under test, turning on said clock and sending a second signal from said device under test to said emulator device;
>
> receiving said second signal at said emulator device;
>
> determining the number of clock signals received at said emulator device since said second signal was received; and
>
> resuming execution of said instructions that are performed in lock-step at said emulator device when said determined number of clock signals received at said emulator device since said second signal was received equals a predetermined value.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

23. In regards to Claim 5,

> 5. The method of Claim 4 wherein said device under test further comprises a microcontroller and wherein said first signal comprises a first bit, said first bit received at a register of said microcontroller to indicate that a sleep function is to be performed.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

24. In regards to Claim 6,

> 6. The method of Claim 5 wherein said emulator device further comprises a Field Programmable Gate Array (FPGA) device.

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

25. In regards to Claim 7,

> 7. For a system that includes a device under test and that includes an emulator device:
>
> a) emulating the functions of said device under test by operating in lock-step fashion with said device under test; and

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

> b) performing a stall operation, comprising:
>
> > b1) said device under test conveying clock signals to said emulator device;
> >
> > b2) upon receiving a first signal that indicates that a stall function is to be performed, initiating said stall function at said device under test;
> >
> > b3) upon receiving said first signal, discontinuing said sending of said clock signals from said device under test to said emulator device; and
> >
> > b4) discontinuing execution of said instructions that are performed in lock-step at said emulator device while said sending of said clock signals is discontinued.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

26. In regards to Claim 8,

> 8. The method according to claim 7 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA), said clock signals further comprising signals from said microcontroller central processing unit clock.

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

27. In regards to Claim 9,

> 9. The method of Claim 8 further comprising: resuming sending of said clock signals from said device under test to said emulator device when said stall function has been completed by said device under test, said emulator device operable upon receiving said clock signals to resume execution of said instructions that are performed in lock-step.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

28. In regards to Claim 10,

> 10. A method for performing a sleep operation, comprising:
>
> executing a sequence of instructions by a device under test, said device under test including at least one clock for generating clock signals;
>
> executing said sequence of instructions by an emulator device emulating the functions of said device under test, said emulator device executing said sequence of instructions in lock-step fashion with said device under test;

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

> receiving a first signal at a register of said device under test that indicates that a sleep function is to be initiated;
>
> initiating said sleep function at said device under test upon receipt of said first signal;
>
> turning off said at least one clock of said device under test; and
>
> discontinuing execution of instructions that are performed in lock-step by
>
> said emulator device upon said turning off of said clock.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

29. In regards to Claim 11,

> 11. The method according to claim 10 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

30. In regards to Claim 12,

> 12. The method of Claim 11 wherein said at least one clock includes a microcontroller CPU clock.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

31. In regards to Claim 13,

> 13. The method of Claim 12 further comprising:
>
> when said sleep function has been completed by said device under test, resuming generation of clock signals at said device under test and coupling said clock signals to said emulator device;
>
> when said sleep function has been completed by said device under test, sending a second signal from said device under test to said emulator device;
>
> receiving said second signal at said emulator device;
>
> determining the number of clock signals received at said emulator device since said second signal was received; and
>
> resuming execution of said instructions that are performed in lock-step at said emulator device when said determined number of clock signals received at said emulator device since said second signal was received equals a predetermined value.

32. In regards to Claim 14,

> 14. The method according to claim 13 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

33. In regards to Claim 15,

> 15. The method of Claim 14 wherein said first signal is a first bit, said sleep function initiated upon the receipt of said first bit at a register of said microcontroller.

Examiner finds that the memory (Fig.7, Item 206) corresponds to claimed register. See col.12, lines 4-11 for more details.

34. In regards to Claim 16,

> 16. A method for performing a stall operation, comprising:
>
> executing a sequence of instructions by a device under test;

> executing said sequence of instructions by an emulator device emulating the functions of said device under test, said emulator device executing said sequence of instructions in lock-step fashion with said device under test;

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

> said device under test sending clock signals to said emulator device; receiving a first signal at a register of said device under test that indicates that a stall function is to be initiated;
>
> initiating said stall function at said device under test upon receipt of said first signal;
>
> discontinuing said sending of said clock signals from said device under test to said emulator device upon initiation of a stall function at said device under test; and
>
> discontinuing execution of said sequence of instructions at said emulator device while said sending of said clock signals is discontinued.

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

35. In regards to Claim 17,

> 17. The method according to claim 16 wherein said device under test is a microcontroller and wherein said emulator device includes a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

36. In regards to Claim 18,

> 18. The method according to Claim 17 wherein said clock signals further comprise signals from a central processing unit clock of said microcontroller.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

37. In regards to Claim 19,

> 19. The method of Claim 18 further comprising: resuming sending of said clock signals from said device under test to said emulator device when said stall function has been completed by said device under test, said emulator device operable upon receiving said clock signals to resume execution of said sequence of instructions.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

38. In regards to Claim 20,

> 20. The method of Claim 19 wherein said sequence of instructions comprises the core processing functions of said microcontroller.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Examiner finds that the RUN/HALT of the target program applies to all processing functions of the target program 22.

39. In regards to Claim 21,

21. An in-circuit emulation system comprising:

a device under test that executes a sequence of instructions, said device under test operable upon receiving a first signal to initiate a stall function;

an emulator device for emulating the functions of said device under test so as to execute said sequence of instructions in lock-step fashion with said device under test, said emulator device receiving clock signals send from said device under test; and

wherein said device under test sends clock signals to said emulator device, said device under test operable upon receiving said first signal to discontinue sending said clock signals to said emulator device, said emulator device is operable to discontinue execution of said sequence of instructions while said sending of said clock signals is discontinued.

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22) will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

40. In regards to Claim 22,

22. The in-circuit emulation system of Claim 21 wherein said device under test is a microcontroller, said microcontroller operable to resume sending said clock signals to said emulator device when said stall function has been completed by said microcontroller, said emulator device operable upon receiving said clock signals to resume execution of said sequence of instructions.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

41. In regards to Claim 23,

> 23. The in-circuit emulation system of Claim 22 wherein said clock signals further comprise signals from a central processing unit clock of said microcontroller.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

42. In regards to Claim 24,

> 24. The in-circuit emulation system of Claim 23 wherein said emulator device comprises a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

43. In regards to Claim 25,

> 25. An in-circuit emulation system comprising;
>
> a device under test that executes a sequence of instructions, said device under test operable upon receiving a first signal to initiate a sleep function at said device under test and operable turn off a clock of said device under test; and
>
> an emulator device for emulating the functions of said device under test so as to execute said sequence of instructions in lock-step fashion with said device under test, said emulator device operable upon turning off said clock to discontinue execution of said sequence of instructions at said emulator device.

Profit teaches (see col.11, lines 28-43) that the controller (Fig.7, Item 228) sets the value of the TIME INTERVAL signal on its dedicated line (Fig.9, Item 262).

Profit teaches (see col.11, lines 37-40) that "This method allows a design engineer to determine how each section of the target program (Fig.7, Item 22)

will be synchronized with the simulation of the target circuitry in the hardware simulator (Fig.7, Item 210)."

Profit also teaches (see col.11, lines 40-42) that "Setting the time interval to zero would cause synchronization to occur at the execution of each instruction."

Profit teaches (See col.9, line 40 to col.10, line 31) that the RUN/HALT controller (Fig.8, Item 240) halts the emulator's processor (Fig.7, Item 204).

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

44. In regards to Claim 26,

> 26. The in-circuit emulation system of Claim 25 wherein said device under test comprises a microcontroller, said device under test operable when said sleep function has been completed by said device under test to turn on said at least one clock and to send a second signal to said emulator device, said emulator device operable upon receiving said second signal to determine the number of clock signals received at said emulator device since said second signal was received and said emulator device operable to resume execution of said sequence of instructions when said determined number of clock signals received at said emulator device since said second signal was received equals a predetermined value.

Profit also teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Profit also teaches (See col.12, lines 24-35) that "Upon receiving the clock synchronization acknowledge circuit, the controller 228 activates the RESET signal on line 258 which causes the target bus watch circuit 224 to release the RUN/HALT signal and allow continued execution of the target program 22."

Since the release of the RUN/HALT signal reactivates the clock, it is inherent that the initial RUN/HALT signal "turned off" the clock, as claimed by the applicant.

45. In regards to Claim 27,

> 27. The in-circuit emulation system of Claim 26 wherein 22 device under test is a microcontroller, said at least one clock further comprising a central processing unit clock of said microcontroller.

Profit teaches (See col.12, lines 24-35) that the both the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) have clock counters.

Moreover, Fig.7 shows that that the hardware simulator (Fig.7, Item 210) and the target program (Fig.7, Item 22) run inside a "processor model shell" (Fig.7, Item 212) and a processor (Fig.7, Item 204). Therefore, the clocks are inherently "internal CPU clocks", because the RUN/HALT signals go to these entities.

46. In regards to Claim 28,

> 28. The in-circuit emulation system of Claim 27 wherein said emulator device comprises a field programmable gate array (FPGA).

Profit teaches (See col.3, line 65 to col.4, line 9; and col.6, lines 20-25) the use of FPGAs as emulator devices.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749.

Any response to this office action should be faxed to (703) 872-9306, or mailed to:

USPTO
P.O. Box 1450
Alexandria, VA 22313-1450

or hand carried to:

USPTO
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

June 26, 2005

L. P. Picard

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100